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Design and Fabrication of 850 and 980 nm Vertical Cavity Surface Emitting Laser

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M. T. Lara and W. Chang

ARL-TR-3187 March 2004

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14. ABSTRACT

Vertical-cavity surface-emitting lasers (VCSEL) are the most suitable light sources for certain optoelectronic applications because of their planner nature of light emission. VCSELs on GaAs substrates were grown by the molecular beam epitaxy technique. In this report we present detailed procedures to design and fabricate 850-nm top-emitting and 980-nm bottom-emitting VCSELs. First a test structure was grown by the molecular-beam epitaxy (MBE) technique and was characterized by reflectance and photoluminescence techniques. We used a wet oxidation process for current confinement in the laser structure. The VCSELs have low threshold current, low voltage drop and hence are suitable for hybridization onto silicon MOS circuits.

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VCSEL, oxidation, surface emitting laser

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1. Introduction

The vertical-cavity surface-emitting laser (VCSEL) is an optoelectronic device having several attractive features, including low power and high modulation frequency. Recently many new design concepts including a narrow trench on the top mirror (*1*) and photonic crystals structure (*2*) have been proposed to achieve single mode operation and better quantum efficiency VCSELs. Large 2-D VCSEL arrays (32×32) have been produced for optical communication circuits. In order to achieve good performance in a VCSEL array, it is required to fabricate devices with low threshold current, low voltage drop and high optical power. The increasing complexity of these vertically integrated structures, together with the precision required in their epitaxial growth, demands a well controlled and reproducible fabrication process. The VCSEL fabrication process involves several etching and deposition steps; all the process steps need to be calibrated before the actual fabrication starts. We present here the complete fabrication process for both 850-nm and 980-nm VCSEL devices.

Generally ion-implantation (*3*) and/or oxidation (*4*) are used for current confinement in VCSEL devices. The oxide confined VCSEL has several advantages over ion-implanted VCSEL. They are: a) full use of top Distributed Bragg Reflector (DBR) low resistance, b) elimination of sidewall non-recombination near the optical cavity, c) minimization of lateral current spreading to outside of laser cavity, d) smaller refractive index of the Al-oxide layer induces index guided optical confinement (*5*). Hence oxide confinement VCSEL has low threshold current, low voltage drop and the highest power conversion efficiency. We used wet oxidation technique for current confinement for both the 850 and 980 nm devices. Threshold current decreases with an increase in oxidation time (*6*) due to reduction in current aperture down to some optimum diameter. We used different mesa sizes in the experiment to determine the effect of oxidation on device threshold current. We found that the threshold current decreases and slope efficiency increases with longer oxidation time. We obtain good agreements between theoretical predications and experimental results for the limited range of mesa sizes used in our experiments.

2. Experimental Procedure

The 850-nm top-emitting VCSEL structure was grown by the MOCVD technique on an n-plus substrate. It has 35 pairs of Si-doped bottom $Al_{.16}Ga_{.84}As$ - $Al_{.9}Ga_{.1}As$ DBR, and a λ cavity consisting of three 70-Å, $Al_{.3}Ga_{.7}As$-GaAs quantum wells (QW). The top DBR consists of 25 pairs of $Al_{.9}Ga_{.1}As$- $Al_{.16}Ga_{.84}As$ p-doped layers. The heavy-hole resonant energy was designed to account for the band gap narrowing at higher carrier injection conditions. This ensures a good

match between the gain spectrum and the cavity mode characteristics. A high Al content ($Al_{.98}Ga_{.02}As$) 300 Å layer was placed both above and below the QW layer for selective lateral oxidation.

The VCSEL processing started with a ring contact Ti/Pt/Au metal deposition as the p-type top contact layer. The detailed fabrication procedure is given in appendix A. An inductively coupled plasma (ICP) etching technique with Cl_2 and BCl_3 gas mixture was used for mesa etching into the semiconductor hetrostructure. The mesa diameters employed varied between 15-34 μm and the mesa height was 4.5 μm. The wet oxidation was carried out at 400 °C at different times with nitrogen carrier gas bubbled through water at 85 °C. The oxide width around the edge of the mesa structure, due to the wet oxidation, varies between 4.0 μm-8 μm. The device mesas were passivated by low-temperature plasma-enhanced chemical vapor deposition (PECVD) of 2000 Å of SiO_2. Spin-coated cyclotene (BCB) resin was used for planarization. After complete curing in a nitrogen environment at 250 °C, the BCB film was back etched in CF_4/O_2 plasma completely from the top of the mesa area. We used an offset interconnect metal contact for flip chip bonding so that the pressure due to flip chip bonding would not be applied to the mesa structure. A Ge/Ni/Au metal film was deposited on the back side as the n-contact layer. Rapid thermal annealing was done at 410 °C for 60 sec. in a nitrogen environment to reduce the contact resistance.

The 980 nm bottom emitting VCSEL epi structure was grown on an n-type GaAs substrate by the MBE technique. The structure has 15 pairs of quarter-wavelength n-bottom DBR layers and a λ cavity consisting of two $In_{.18}Ga_{.82}As$-GaAs quantum wells, and 32 pairs of layers in the p-doped top DBR. Two 300-Å high-Al-content ($Al_{.98}Ga_{.02}As$) layers were placed one above and one below the quantum well region. Test wafers with a similar structure were repeatedly grown and characterized by photo reflectance and photoluminescence spectroscopy until the precise desired growth condition and epitaxial structure were achieved.

The device fabrication for the 980 nm VCSEL started with a Ti/Pt/Au circular dot metal deposition for the p-type contact. The mesa area was photo lithographically patterned and etched by a Cl_2/BCl_3 ICP dry etching technique at room temperature. The mesa diameters used in the study varied between 16-38 μm and the mesa height was 5.0 μm. Wet oxidation was carried out at 405 °C at different times with nitrogen carrier gas bubbled through water at 85 °C. The mesas were passivated by low-temperature plasma-enhanced chemical vapor deposition (PECVD) of 2000 Å of SiO_2. Spin coated cyclotene (BCB) resin was used for planarization. A Ge/Ni/Au metal film was deposited outside the laser emission area on the back side of the wafer as n-contact layer. Rapid thermal annealing was done at 410 °C for 60 sec. in a nitrogen environment as the final processing step in the device fabrication procedure. A detailed fabrication process sequence for the 980-nm VCSEL is given in Appendix B.

3. Results and Discussion

The typical growth rate for the GaAs VCSEL hetrostructure was about 1.0 micron/hour. Hence the growth rate had to be accurately calibrated before the actual VCSEL wafer was grown. In Figure 1, the theoretical reflectance curve of a test structure with bottom mirror and cavity structure only is compared with experimental curve. In this test structure the top mirror is replaced by a phase matching layer, so that both the quantum well and cavity resonance peaks in the reflectance curve can be observed. The QW peak was designed approximately 15 meV higher than the cavity peak so that the band narrowing due to the carrier injection and the heat will shift maximum of the gain spectrum to match with cavity resonance. By comparing the experimental result with the theoretical curve, we found that the position of the heavy hole peak is in good agreement with the theory, while the wavelength of the cavity resonance peek is 1% shorter than the theoretical value. Hence the experimental curve needs about 1% higher growth to match with theoretical curve. Accordingly, when the actual VCSEL wafer was grown, the necessary correction in growth parameter was carried out. Although the required correction could be either changing the flux rate by varying the source temperature or by changing the deposition time, the later correction is preferable.

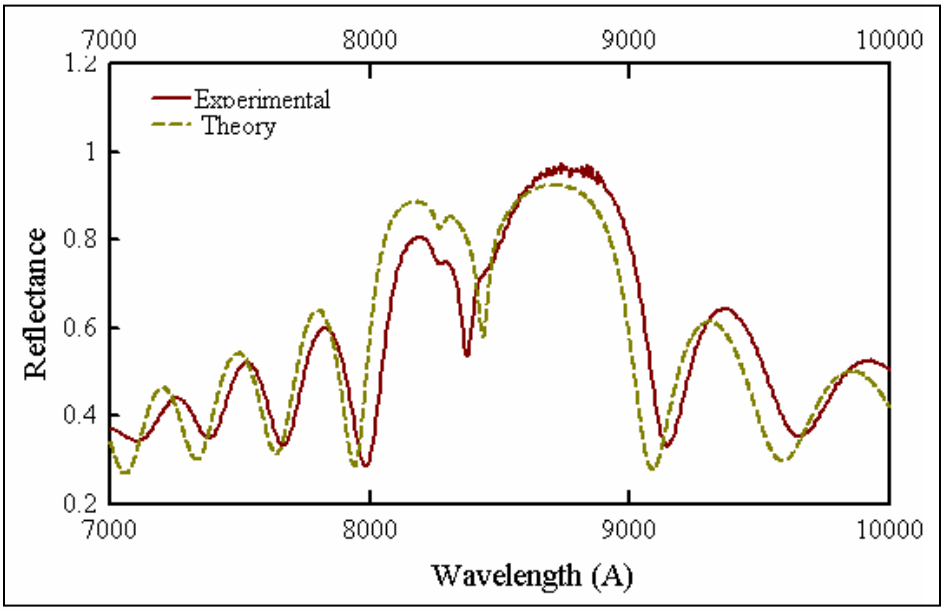

Figure 1. Theoretical and Experimental reflectance curve from 850 nm test structure.

In case of reflectance from a complete VCSEL structure, only the cavity resonance is seen, as depicted in Figure 2. The theoretical spectra has a peak at 8500 Å where as the experimental curve has peak at 8400 Å. It is observed that so long as both the experimental and theoretical curves are within 1% of the design value, the wafer is suitable for laser emission. This should not

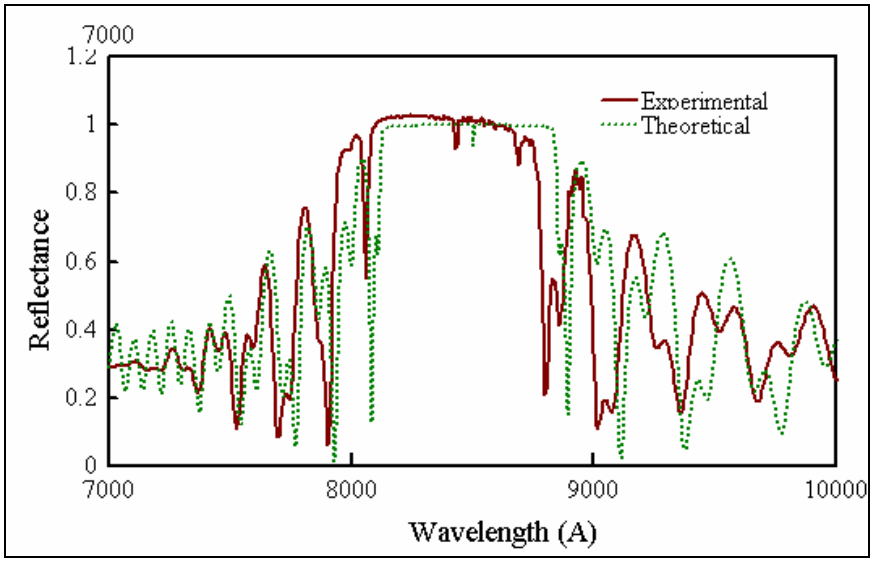

Figure 2. Theoretical and experimental reflectance spectra from 850 nm VCSEL structure.

be confused with our statement in above paragraph, which states that 1% of higher growth should be made, compared to experimental calibration sample. The calibration sample has a lesser number of epi layers than the full VCSEL structure, and hence stringent calibration procedures should be followed. The spectra taken here are taken here from the wafer number 1333 grown in Gen II MBE machine.

In case of 980-nm VCSEL, we observed a good agreement between theoretical and experimental curves as seen in Figure 3. The theoretical curve has a small cavity resonance peak at 9800 Å. Since the 980 nm VCSEL is designed for bottom emitting source, we did not see any peak in experimental reflectance curve as it was taken from front side of the wafer. This wafer has 32 mirror pairs in the top side and 15 pair in the bottom side of the cavity. However, we observed (not shown here) a peak at 970 nm when the reflectance was taken from the bottom side of the wafer.

One of the important process steps in VCSEL fabrication which needs calibration is the wet oxidation step. The wet oxidation rate depends on many parameters including, oxidation temperature, water bubbler temperature, gas flow rate and also the thickness of the AlAs oxidation layer. The thinner the AlAs oxidation layer, the higher the oxidation rate (*6*). However there exists a minimum thickness of 150 Å for AlAs layer below which no appreciable oxidation occurs. Oxidation rate also slightly depends on doping type and concentration in the oxidation layer (*7*). First we calibrated the oxidation process by oxidizing at different furnace temperatures. We used 300 Å of AlAs layer both below and above the QW region. In Figure 4, the SEM picture of cross-sectional view is seen with two oxidation layers, one above and another below the QW cavity region. It is also seen that small oxidation occurs in the top and bottom mirror.

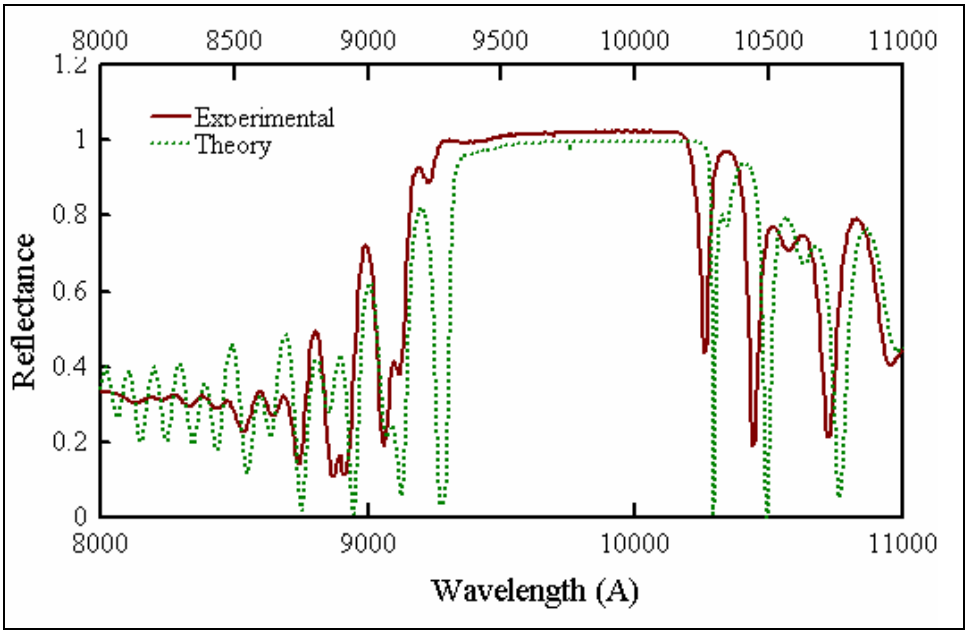

Figure 3. Experimental and theoretical photo reflectance plots of 980 nm VCSEL structure.

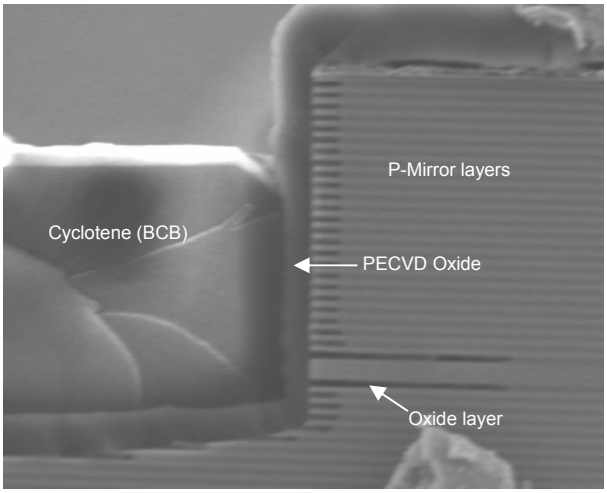

Figure 4. SEM picture of the cross-sectional view of VCSEL after 40 min oxidation at 400 C.

However, the oxidation rate in the mirror layer is much lower compared to the AlAs oxidation layer. In this figure we used the 850-nm VCSEL wafer. We used cyclotene (BCB) film for planarization. As seen in this figure, BCB film is very close to the top of the mesa region and hence suitable for planarization. We used 2000 Å of PECVD oxide to improve the adhesion between the GaAs substrate and BCB film. Low temperature oxide film was deposited using a plasma therm 790 PECVD system at 250 C. Since wet oxidation creates negatively charged traps, in the bulk of the oxide we carried out an experiment to anneal the devices in nitrogen

environment. A large (18%) increase in light output is observed by annealing the devices at 400 C for one hour (*8*).

The top view optical micrograph of 850-nm top emitting VCSEL processed chip is shown in Figure 5. As shown, the device has a clear circular area where the light is emitted. Indium bump was deposited on the offset pad area for flip chip onto CMOS driver circuit. The offset bump helps in reducing strain on actual mesa area. The picture is taken after the BCB planarization and hence, metal film is in plane with the top of the VCSEL mesa area.

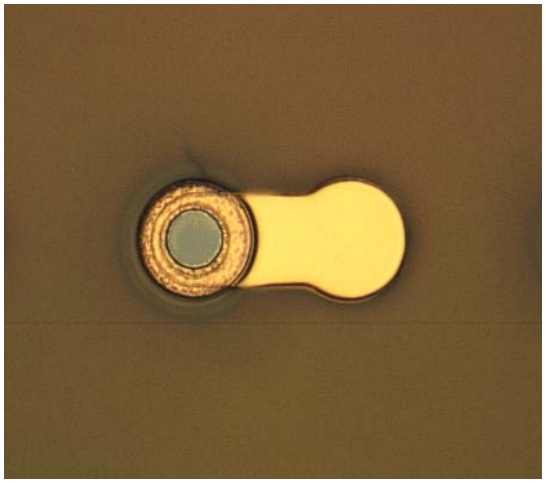

Figure 5. Photograph of processed chip.

The current-light-voltage (ILV) curve for 850-nm VCSEL from wafer number 1333 is shown in Figure 6. The devices have been oxidized for 40 minutes and hence have optical aperture of 4 and 16 micron for 20 and 32 micron mesa respectively. The threshold current decreases with decrease of aperture size. The maximum optical power for 20 and 32 micron mesa devices are 0.4 and 3.8 mW respectively. The light power is comparatively lower from other wafer (we got much higher power from Luxnet wafer). We believe the output power will be improved with an increase of oxidation aperture and the reduction of top mirrors. The slope efficiency is approximately 0.6 W/A, which is comparable to the state of the art devices from semiconductor foundries. The voltage drop on these devices is about 3.0 V near the threshold of laser emission. Hence these devices are suitable for flip chip bonding onto CMOS driver circuit with operating voltage of 5.0 Volt. However, we believe the voltage drop will be improved with carbon doping incorporated into MBE system.

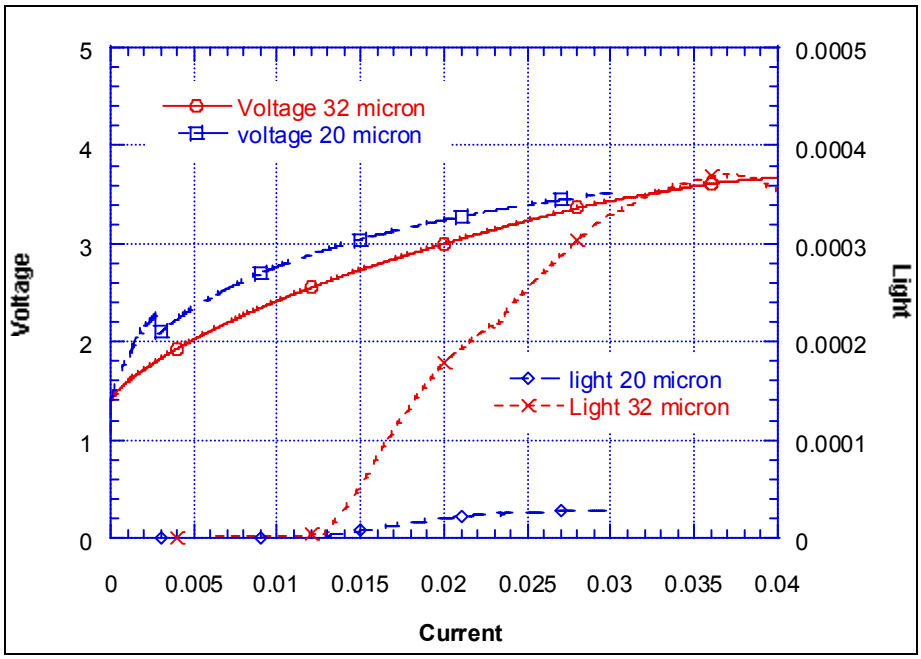

Figure 6. ILV of different mesa size devices.

In Figure 7, the experimental ILV curves for 980-nm devices are plotted. As predicted, both threshold current and maximum light output decrease with mesa size. The ILV measurement was done by probing p-metal dot on the top of the mesa structure with the original mesa diameter of 30 micron. In the actual 8×8 array we use offset bump for flip chip bonding. The aperture sizes after 20, 30 and 40 minutes of oxidation are 18, 12 and 6 micron respectively. As predicted, the voltage drop on the device increases with the decrease of aperture sizes as the resistance of the mesa structure increases with each decrease of mesa diameter. The bottom metal layer was deposited with back side alignment keeping the emitting region clear for light emission. Both top and bottom metal layer thickness and composition are the same for 850-nm and 980-nm devices. The voltage drops in these devices are comparatively higher and we hope with carbon doping, in the future, voltage drop will be reduced.

The light-current-voltage (L-I-V) curves for 980 nm VCSEL with 40 minutes oxidation of different sizes are seen in Figure 8. The current aperture for 26, 28, and 36 micron after the oxidation were 2, 4 and 12 micron respectively. We achieved sub-mille ampere threshold current for 2 micron aperture devices. The maximum light output decreases, while slope efficiency increases with each decrease in mesa diameters. The voltage drops increase with each decrease of mesa diameters as the resistance of mesa area increases. The roll-off of light power after attaining its maximum value is due to thermal heating effect.

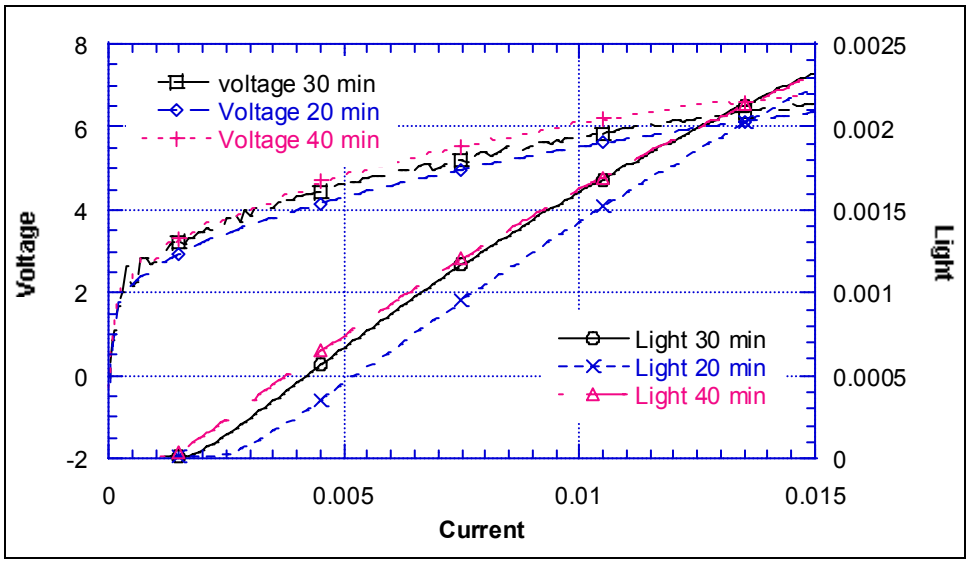

Figure 7. ILV of 980 nm VCSEL with different oxidation time.

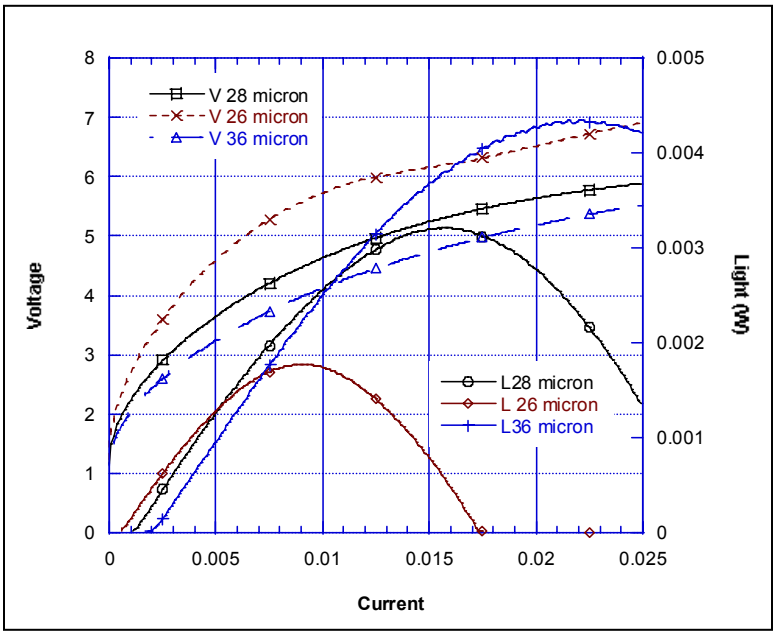

Figure 8. ILV of different mesa devices after 40 min. of oxidation.

4. Conclusions

This report contains detail design, fabrication procedure and device characteristics of 850-nm and 980-nm VCSELs. The device ILV characteristics are similar to the characteristics of state of the art devices from VCSEL foundries. Photo reflectance data is required to calibrate the epitaxial structure. The device characteristics of oxide confined VCSEL is superior to VCSEL with unoxidized mesa structures. Low threshold current VCSEL with low turn-on voltage can be useful for flip chip bonding onto CMOS driver circuits.

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Appendix A

Step	Process
Wafer	One cm square top emitting 850 nm material
P-Contact	Spin Coat AZ 5214IR 4 KRPM 30 sec. Expose 1.5 sec **P ring mask** Develop 1:1 AZ 312:H_2O 40 sec. Rinse in water E-beam deposition (300 Ang Ti/300 Ang. Pt/2500 Ang. Au) and liftoff in Acetone
Mesa Etch	Clean in Acetone/ Methanol/ H_2O Spin SC 1827 PR at 4 KRPM for 30 sec. Expose **Mesa 1 mask** Develop in 312 dev. For 1 min. Dry etching in Cl2 plasma 4.5±.1 micron
Oxidation	Oxidize at 400 C in wet oxidation furnace for different times
Oxide deposition	Deposit 2000 Ang. of silicon dioxide by PECVD method
Cyclotene deposition	Spin Adhesion promoter at 1000/10sec and then ramp to 4000 rpm for 30 sec. Spin Cyclotene 3022-46 resin onto the wafer just after adhesion promoter. Speed 3000 rpm/30 sec 5 min ramp to 50 C, hold for 5 min 15 min ramp to 100 C 15 min hold 15 min ramp to 150 C, hold 15 min 30 min at 210 C (partial cure) N2 environment
Planarization	RIE etch at 150 Watt with 80%O2 and 20% CHF3 for 7-8 min.
Metal	Spin AZ 5214 IR, at 4 KRPM for 40 sec. Expose 1.5 sec, **Metal mask** Develop 1:1 AZ 312:H_2O 40 sec. Ebeam deposition (Ti 300 ang./3000 Ang. Au) and Liftoff
N- Metal	Spin AZ 5214 IR, at 4 KRPM for 40 sec.

	Expose 1.5 sec, **Metal 2 mask** Develop 1:1 AZ 312:H_2O 40 sec. On back side E-beam deposit (50 Ang. Ni/300 Ang. Au /100 Ang. Ni / 3000 Ang. Au)
Indium	Spin 4620, at 4 KRPM for 40 sec. Expose **Indium mask** Chlorobenzene soak for 10 min. Develop 1:3 400K:H_2O 2 min. PR thickness should be 7.25 micron Ebeam deposition (300 Ang./ 5 micron.. Indium with 30 Ang./sec rate) Liftoff

Appendix B

Process	Take two pieces of 980 nm VCSEL wafer
P-contact	Spin Coat AZ 5214IR 4 KRPM 30 sec. Expose **Mesa mask** Develop 1:1 AZ 312:H_2O 40 sec. Rinse in water E-beam deposition (300 Ang Ti/300 Ang. Pt/2500 Ang. Au) liftoff in Acetone RTA at 405 C for 60 sec.
Mesa Etching	Clean in Acetone/ Methanol/ H_2O Spin SC 1827 PR at 4 KRPM for 30 sec. Bake at 90C for 30 min. in oven Expose for 8 sec. **Mesa 1 mask** Develop in 312 dev. For 1 min. Hard bake at 120 C for 35 min. Dry etching in Cl2 plasma 5.3 micron
N-Contact	On back side E-beam deposit (50 Ang. Ni/300 Ang. AuGe /100 Ang. Ni / 3000 Ang. Au)
Oxidation	Clean photo resist in Acetone/methanol/H_2O Oxidize at 400 C in wet oxidation furnace for different times
Passivation	Deposit 2000 Ang. of Silicon dioxide by PECVD method
Cyclotene	Spin Adhesion promoter at 1000/10sec and then ramp to 4000 rpm for 30 sec. Spin Cyclotene 3022-57 resin onto the wafer just after adhesion promoter. Speed 3000 rpm/30 sec 5min ramp to 50 C, hold for 5 min 15 min ramp to 100 C 15 min hold 15 min ramp to 150 C, hold 15 min 60 min at 250 C in N2 environment
Planarization	RIE etch at 150 Watt with 80%O2 and 20% CHF3 for 7-8 min.
PECVD Deposition	Deposit 2000 Ang. SiO_2 by PECVD method Spin AZ 5214 IR at 2 KRPM for 40 sec Expose 3 sec. **Nitride mask**

	Develop 1:1 AZ 312:H_2O 40 sec. Etch oxide from mesa area
Interconnect metal	Spin AZ 5214 IR, at 4 KRPM for 40 sec. Expose **Metal mask** Develop 1:1 AZ 312:H_2O 40 sec. Ebeam deposition (Ti 300 ang./3000 Ang. Au) and Liftoff
Indium deposition	Spin 4620, at 4 KRPM for 40 sec. Expose **Indium mask** Chlorobenzene soak for 10 min. Develop 1:3 400K:H_2O 2 min. Ebeam deposition (300 Ang./ 5 micron.. Indium with 30 Ang./sec rate) Liftoff

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